Remarks

I. Summary of the Examiner's Objections

In the Office Action mailed July 17, 2002, the Examiner subjected claims 1-59 of the application to a restriction requirement. On page 2 of the aforementioned Office Action, the Examiner grouped claims 1-31 as drawn to a circuit for quantifying a high voltage signal; claims 32-54 and 59 as drawn to a high voltage amplifying circuit utilizing a current differencing circuit; and claims 55-58 as drawn to a high voltage amplifying circuit utilizing a current steering circuit.

II. Election

Applicant hereby elects to proceed with the invention as defined in group 1 (claims 1-31) in the instant application.

III. New Claims

Claims 60 – 76 are added for the consideration of the Examiner and are submitted to be consistent with the elected group of claims.

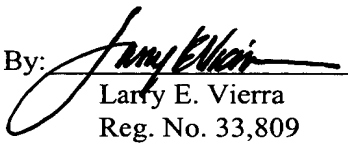
IV. Proposed Figure Correction

Included herewith is a proposed correction to Figure 4a showing the correct placement of the bracket. A clean copy of the revised drawing is included.

In view of the foregoing, Applicant respectfully asserts that the present application is in condition for examination. Should the Examiner have any questions with regard to the instant response, the Examiner is respectfully requested to contact the undersigned attorney.

Respectfully submitted,

Date: September 16, 2002

By: 
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APPENDIX

Below are the marked-up copies of the amended claims.

1. (Amended) A circuit for quantifying a high-voltage signal comprising:

a first [high-voltage input] terminal having a first voltage;

an output terminal;

a field transistor having a drain, a gate, and a source, said gate connected to said [high-voltage input] first terminal, said drain and source having a second and third voltage, said output terminal coupled to said [drain] field transistor;

wherein said output terminal provides a signal representative of said first voltage.

12. (Amended) The circuit as defined in claim 2 wherein said field transistor further includes a drain extension region formed under said gate oxide by a dopant species introduced before said LOCOS step [in a region absent of said silicon-nitride].

14. (Amended) A circuit, comprising:

at least one low voltage input;

a[t least] first [one] high voltage terminal; and

a first field transistor having a source, a drain and a control region;

wherein said control region is coupled to said first high voltage terminal.

21. (Amended) The circuit of claim 14 wherein said field transistor comprises a MOS transistor having an oxide separating said source and said drain regions and said control region, and said oxide has a thickness greater than the maximum thickness available to other MOS devices on an integrated circuit chip on which the circuit is manufactured.

27. (Amended) The circuit of claim 25 wherein said first high voltage terminal has a swing of at least 40 v.

60. (NEW) The circuit as defined in claim 1 wherein said signal representative of said first voltage is a voltage signal.

61. (NEW) The circuit as defined in claim 1 wherein said signal representative of said first voltage is a current.

62. (NEW) The circuit of claim 1 further including a low-voltage input, wherein said first terminal includes an amplified representation of said low-voltage input.

63. (NEW) The circuit of claim 15 further including a current-differencing circuit coupled to said first field transistor and said second field transistor, said current-differencing circuit having an output.

64. (NEW) The circuit of claim 63 further including a trans-impedance stage having an input and an output, said trans-impedance stage input coupled to said current-differencing circuit output.

65. (NEW) The circuit of claim 63 said current-differencing circuit further including:

a first input current;

a second input current;

wherein said output of said current-differencing circuit includes an amplified signal representative of the difference between said first input current and said second input current.

66. (NEW) The circuit of claim 14 wherein said first high voltage terminal includes an amplified representation of said low voltage input.

67. (NEW) The circuit of claim 14, further including:
a second high voltage terminal; and
a differential mode feedback circuit.

68. (NEW) The circuit of claim 67 wherein the voltage between said first high voltage terminal and said second high voltage terminal includes an amplified representation of said low voltage input.

69 (NEW) The circuit of claim 67 further including a common mode feedback circuit.

70. (NEW) The circuit of claim 14 further including
a reference circuit;
a current-steering circuit having an input and an output.

71. (NEW) The circuit of claim 68 wherein said current-steering circuit further includes a coupling from said low-voltage input to said input, and said current steering circuit is coupled to said reference circuit.

72. (NEW) The circuit of claim 69 wherein said reference circuit further includes a second field transistor having a gate and a reference voltage connected to said second field transistor gate.

73. (NEW) The circuit of claim 68 further including a differencing circuit having a first input, a second input, and an output, said first input coupled to said first field transistor and said second output coupled to the output of said current-steering circuit.

74. (NEW) The circuit of claim 14, further comprising at least one MEMS mirror coupled to said high-voltage terminal.

75. (NEW) A high-voltage amplifier comprising:

a first terminal receiving a low voltage;

a second terminal;

a first field transistor having a gate, a source, and a drain, the field transistor gate being coupled to the second terminal output;

a reference circuit;

a current-steering circuit having an input and an output coupled to said reference circuit.

76. (NEW) The amplifier of claim 75 wherein the reference circuit includes at least a second field transistor.

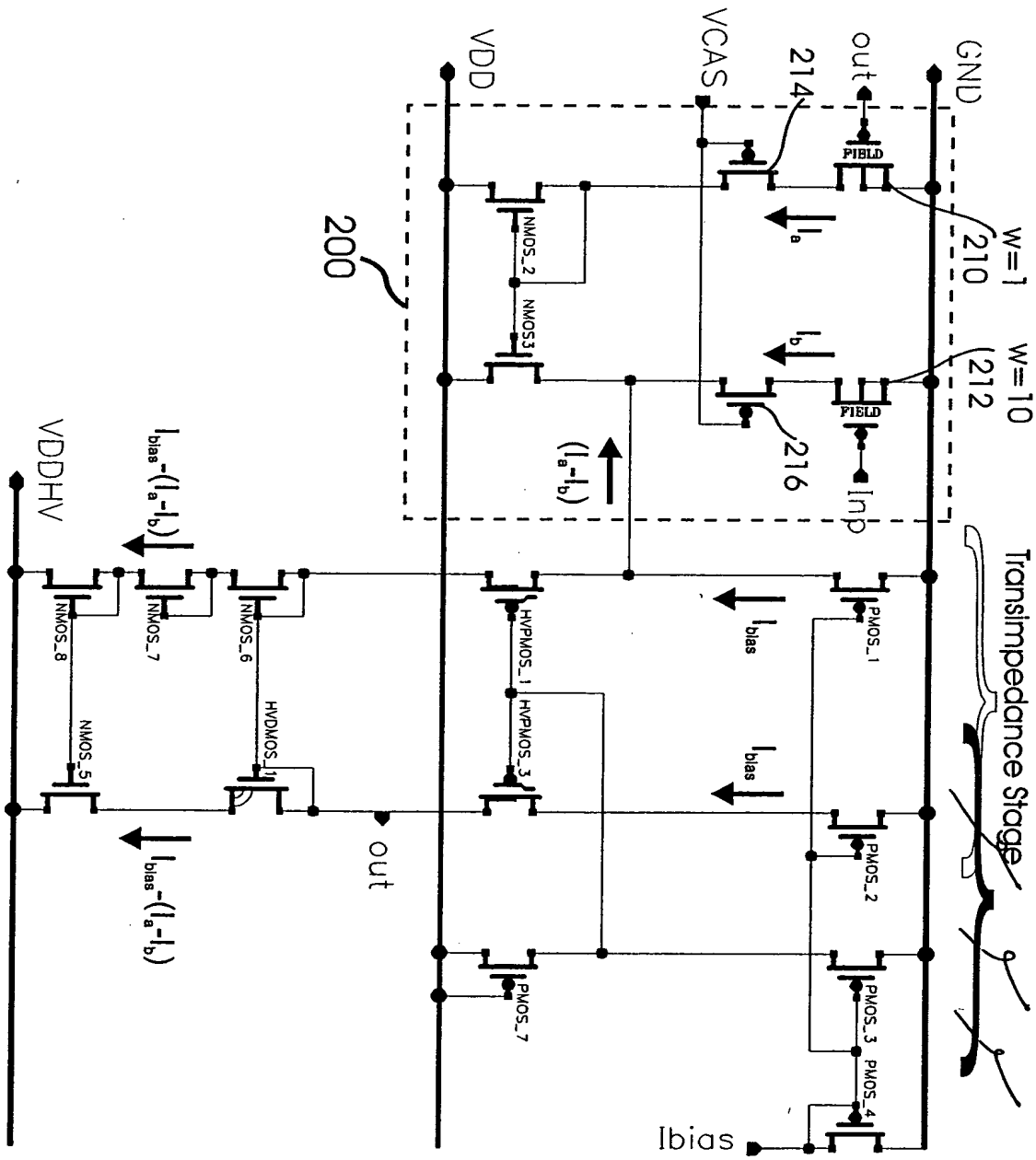

Figure 4a